



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,351	02/26/2004	Ignazio Martines	61181-00013USPX	9082
23932	7590	04/28/2006	EXAMINER	
JENKENS & GILCHRIST, PC				NGUYEN, NAM THANH
1445 ROSS AVENUE				ART UNIT
SUITE 3200				PAPER NUMBER
DALLAS, TX 75202				2824

DATE MAILED: 04/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/789,351	MARTINES ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Nam T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 10 March 2006.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 1-5 is/are allowed.
- 6) Claim(s) 6,7,9,10,12,13 and 15-20 is/are rejected.
- 7) Claim(s) 8,11,14 and 21-23 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 26 February 2004 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: EAST search update.

## DETAILED ACTION

1. The amendment filed on 3/10/06 has been entered.

Claims 1-23 are pending in the application.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 6-7, 9-10, 12-13, 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hoang (U. S. Patent No 5,852,578).

Regarding claim 6, figure 9 of Hoang discloses a non-volatile memory circuit comprising a non-volatile memory cell (FG1, FG2, FG3, FG4) coupled to a bit line (81, 83) and a word line (WL1, WL2); and a selectively actuated current sinking conduction to ground path (T5) coupled to the bit line (81 and 83).

Regarding claim 7, the memory cell of Hoang comprises a floating gate (14, figure 1) transistor having a drain terminal (15, figure 1) connected to bit line (81, figure 9) and its gate (16, figure 1) connected to word line (WL1 and WL2).

Regarding claim 9, since every memory device must have a row decoder (connected to word line) and column decoder (connected to bit line), then the reference of Hoang inherently includes a column decoder, and such decoder is connected to bit

line. Therefore, the conduction path to ground (T5) is coupled to the bit line through column decoding circuit.

Regarding claim 10, wherein the selectively actuated conduction to ground path (T5) is coupled to the bit line (81) through at least a bit line biasing circuit (T3).

Regarding claim 12, figure 9 of Hoang discloses a memory matrix (FG1-FG4) including a plurality of memory cells (FG1, FG2) arranged in columns, each associated with a bit line (81), and rows (FG1 and FG1 form a row, FG3 and FG4 form another row), each associated with a word line (WL1, WL2); a column programming circuit (T3) coupled between a programming voltage source (Vcc) and each bit line (81) and activated in response to a first control signal (VPULLUP); and a bypass path circuit (T5) for each bit line (81) and coupled between the programming voltage source (Vcc) and ground and activated in response to a second control signal (VBIAS).

Regarding claim 13, the applicant is referred to the rejection applied to claim 7 for the reasons of this rejection.

Regarding claim 15, the applicant is referred to the rejection applied to claim 9 for the reasons of this rejection.

Regarding claim 16, the bypass path circuit comprises a pass transistor (T5) for each column coupled between the programming voltage source (Vcc) and ground.

Regarding claim 17, figure 9 of Hoang discloses a voltage regulation system for a non volatile memory including a memory cell matrix (FG1-FG4) organized in cell rows (FG1 and FG2) and columns (FG1 and FG3), comprising a program load circuit (T3) for

Art Unit: 2824

each matrix column that biases each memory cell (FG1-FG4) in a selected matrix column with a predetermined voltage value (Vcc) during a programming operation; and a current sinking conduction-to-ground path (T6) for each matrix column, each path being enabled when its associated matrix column is not selected during the programming operation. To be more specific, the non selected bit line is grounded in the programming mode. See column 4, lines 8-11.

Regarding claim 18, the applicant is referred to the rejection applied to claim 7 for the reasons of this rejection.

Regarding claim 19, the applicant is referred to the rejection applied to claim 9 for the reasons of this rejection.

Regarding claim 20, the conduction to ground path in Hoang includes a controlled active element comprising a pass transistor (T5) receiving on a control terminal (the gate of transistor T5) thereof a first enabling signal (VBIAS).

***Allowable Subject Matter***

4. Claims 1-5 are allowed.
5. Claims 8, 11, 14, 21-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior of record fail to teach or suggest a voltage regulation system comprising a program load circuit that is connected in parallel with a current sink (claim 1); a conduction ground path that is connected in parallel with a bit line biasing circuit (claim 8); the bit line biasing circuit and the actuated conduction to ground path are oppositely activated (claims 11, 14, 21), wherein the conduction to ground path is a redundant current path (or dummy current path) to the program load circuit (claims 22 and 23).

### ***Response to Arguments***

6. Applicant's arguments with respect to claims 6-23 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

Art Unit: 2824

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nam T. Nguyen whose telephone number is (571) 272-1878. The examiner can normally be reached on 8 am to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nam T Nguyen  
Examiner  
Art Unit 2824

4/19/06

